

REMARKS

Claims 1-53 are pending.

In responding to the Examiner's prior art rejections, Applicant here only justifies the patentability of the independent claims. As the Examiner will appreciate, should these independent claims be patentable over the prior art, narrower dependent claims would also necessarily be patentable. Accordingly, Applicant does not separately discuss the patentability of the dependent claims, although it reserves the right to do so at a later time if necessary.

The Examiner has rejected all of the non-allowed independent claims (1, 5, 11, 15, 22, 26, 30, 33, 37, 41, 46)¹ as anticipated by USP 6,725,388 ("Susnow"). In this rejection, the Examiner analogizes Susnow's receiver 683 (Fig. 7) to Applicant's receiver; Susnow's decoders 1001-1003 (Fig. 10) to Applicant's decoder; and Susnow's register 810 (Fig. 8) to Applicant's output timing register.

The Applicant respectfully disagrees with the Examiner's conclusions that these components of Susnow meet Applicant's claim limitations.

As the Examiner will note, each of Applicant's rejected independent claims specify (using different language) the idea of receiving signals (e.g., at the receiver) in a first timing domain, decoding the signals (e.g., with a decoder), and outputting decoded signals (e.g., using an output timing register) in a second timing domain.

But the components in Susnow all operate in accordance with a single timing domain. In Susnow, register 683 (Fig. 7) sends signals to the decoders 1001-1003 (Fig. 10), which then send the signals to the transmitter 684 (Figs. 7 and 12). As just noted, this all occurs within a single timing domain (the receiver clock domain). This is verified by Fig. 8, which shows the details of Susnow's elastic buffer 682, which ultimately provides the signals to Susnow's receiver 683. As disclosed in Figure 8, the timing domain dividing line occurs at Susnow's register 810 (which the Examiner analogizes to Applicant's output timing register), dividing the "link clock domain" from the "receiver clock domain." To the right of this dividing line (i.e., in the directions that the

¹ Independent claim 50 has been allowed by the Examiner.

signals flow), the signals encounter the receiver 683 (Fig. 7), then the decoder (Fig. 10), and then ultimately, the transmitter 684 (Figs. 7 and 12), with no change in timing domain.

With this understood, it is clear that Susnow's receiver 683, decoders 1001-1003, and transmitter 684 are all governed in accordance with a single time domain, which does not meet any of Applicant's non-allowed independent claims.

The Examiner tries to incorporate Susnow's register 810 (Fig. 8), analogized to Applicant's output timing register, into the mix to help show Applicant's claimed shift between the two timing domains, but this component is not consistent with the other components identified by the Examiner. As just noted, the signals in Susnow flow from left to right. Thus, the signals from Susnow's receiver 683 go to the decoders 1001-1003 and to the transmitter 684 (Fig. 7 and 12); they do not go to Susnow's register 810, as the Examiner contends.

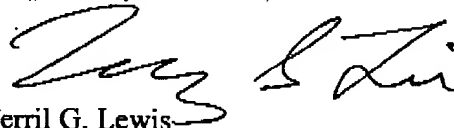
In short, Susnow's register 810 does not receive decoded signals from Susnow's decoders 1001-1003. In the language of claim 1, for example, Susnow's register 810 does not "output[] the at least one decoded signal [from decoders 1001-1003] in a second timing domain." Instead, what receives the decoded output in Susnow is transmitter 684, which as noted above, is in the same timing domain as Susnow's receiver 683.

Therefore, neither claim 1, nor any other non-allowed independent claim, are met by Susnow, and therefore Susnow does not anticipate Applicant's non-allowed independent claims.

The Applicant submits that pending claims 1-53 are patentable over the prior art of record, and requests that a Notice of Allowance issue for these claims.

Please feel free to contact the undersigned with any questions relating to this submission.

Respectfully submitted,



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